ABSTRACT

A packet processing system architecture and method are provided. According to one implementation, the system can include a first and second memory elements and a processor. The first memory element may be utilized for storing: A plurality of packet quality of service indicators; A first packet quality of service field; and A second packet quality of service field. The second memory element is utilized for storing a plurality of second packet quality of service indicators. The processor is operatively coupled to the memory elements for receiving quality of service commands, wherein the service commands include a plurality of third packet quality of service indicators. The processor uses an index to search the second memory element and the search returns a subset of the plurality of second packet quality of service indicators. The index may be the egress marking set or a queue number. The processor then creates a modified data packet by determining which of the packet quality of service fields to insert in the data packet, wherein the determination is based on the one or more quality of service commands.